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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,448	10/26/2004	Hiroshi Takahara	260595US2PCT	4259

22850 7590 07/29/2010

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EXAMINER	
ABDIN, SHAHEDA A	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
07/29/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/511,448	TAKAHARA ET AL.	
	Examiner	Art Unit	
	SHAHEDA A. ABDIN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) *1-9,13 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-12,15 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The correspondence field on 09/25/2009 has been entered and considered by Examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 10, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (US Patent No: 6274887).

Regarding claim 10:

Yamazaki teaches an EL display apparatus comprising:

a substrate that contains a display area having pixels arranged in a matrix, each pixel including an EL element;

a source driver IC (TFT 5002) that is mounted on the substrate and configured to apply a programming current or voltage to the pixels;

a cathode supply line (cathode voltage supply line 5003a) that applies a cathode voltage and is formed on the substrate and located under the source driver IC (5005);

a common cathode line (5006) that is electrically connected to the cathode supply line wiring and formed between the source driver IC and the display area; and

a cathode wiring (cathode wiring for 5007) that branches branching from the common cathode line and is configured to apply the cathode voltage to the pixels in the display area, a potential (voltage) of the cathode supply line being applied to both ends of the common cathode line, and a current being to the EL elements via the cathode anode wiring (column 34, lines 38-67, Fig. 29 A).

Regarding claim 12:

Yamazaki ('4887) further discloses driver transistors (transistors corresponding to drive EL elements, i.e. 5002, 5004) that are configured to apply light-emitting currents to the respective pixels, the driver transistors being P-channel transistors, and transistors configured to generate the programming current in the source driver IC being N-channel transistors (column 30, lines 19-29, Fig. 25 B, and column 34, lines 38-55).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 15, 18- 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US Patent 6274887) in view of Yamazaki (US Patent No: 6765549) .

Claim15:

Yamazaki ('4887) in Fig. 19 A-B discloses an EL display apparatus comprising: a substrate that contains a display area having pixels arranged in a matrix, each pixel including an EL element (5007);

a source driver IC (5002, Fig. 29 A) that is mounted on the substrate and configured to a programming current or voltage to the pixels (column 34, lines 3037, and Fig. 29 B);

; Note that Yamazaki ('4887) discloses an anode of the EL element (i.e. 5007) but, Yamazaki ('4887) does not disclose an anode supply line that applies an anode voltage and is formed on a substrate and located under source driver IC , a common anode line that is electrically connected to the anode supply line and formed between the source driver IC and the display area; and an anode wiring that branches from the common anode line and is configured extends to apply the anode voltage to the pixels in the display area, a potential of the anode supply line being applied to both ends of the

common anode line, and a current being applied to the EL elements via the anode wiring.

Yamazaki ('5549, in Fig. 8A) discloses an anode supply line (1203) that applies an anode voltage and is formed on a substrate and located under source driver IC (1204) a common anode line (1220) that is electrically connected to the anode supply line (1203) and formed between the source driver IC and the display area; and

an anode wiring that branches from the common anode line (1220) and is configured extends to apply the anode voltage to the pixels (e.g. different pixel 1210) in the display area, a potential (Vout) of the anode supply line being applied to both ends of the common anode line, and a current being applied to the EL elements via the anode wiring (column 17, lines 18-35).

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporated the anode supply line and corresponding voltage and a common anode line with associated anode voltage as taught by Yamazaki ('5549) in to the EL display apparatus of Yamazaki ('4887) so that an anode supply line could be applied an anode voltage which being formed on a substrate and located under source driver IC , a common anode line could be electrically connected to the anode supply line and formed between the source driver IC and the display area; and an anode wiring could be branched from the common anode line and is configured extends to apply the anode voltage to the pixels in the display area, a potential of the anode supply line

could be applied to both ends of the common anode line, and a current being applied to the EL elements via the anode wiring. In this configuration the system would provide a high efficient EL device with preventing the decrease in the brightness of an EL element (Yamazaki ('5554) column 4, lines 10-13).-

(3) Regarding claim 18:

Yamazaki ('4887) discloses a switch circuit (i.e. Switching TFT 4102, Fig. 26) that is arranged in an output stage of the source driver IC and configured to turn on and off an output of the programming current or voltage (column 31, lines 30-50).

(4) Regarding claim 19:

Yamazaki ('4887) further discloses the pixel includes a driver transistor (5005, Fig. 29B) applying a current to the EL element (5007), a switching transistor (i.e. connected to El element 5007) applying, to the driver transistor, a signal applied to a source signal line, and a capacitor (capacitor at 5004, Fig. 29B) placed between a gate terminal of the driver transistor and an output terminal of the switching transistor (column 34, lines 38-65, column 35, lines 5-22).

(5) Regarding claims 20 and 23:

Yamazaki ('4887) further discloses wherein the pixel includes a driver transistor (5005, Fig. 29c) applying a current to the EL element (5007), and

a switching transistor (switching transistor corresponding to the EL element) on a current path, and the current is controlled by turning on and off the switching transistor

to generate strip-like non-display areas and strip-like display areas in the display screen (see the illustration in Fig. 27 for stripe like display are) wherein the stripe like non display area and stripe-like display area are generated in the display area and the strip-like non-display area; and the strip-like display area moving in a top-to-bottom while images are display (column 17, lines 4-23, column 31, lines 30-50).

(6) Regarding claim 21:

Yamazaki ('4887) further discloses wherein the display area is configured with red pixels, green pixels, blue pixels and white pixels, each being arranged in a matrix (column 32, lines 42-45).

Regarding claim 22:

Yamazaki ('4887) discloses the display area is configured with pixels of a first color and pixels of a second color, each being arranged in a matrix, and the pixel of the first color having a different size from the pixel of the second color (column 32, lines 42-45).

Regarding claim 24:

Yamazaki ('4887) discloses a detector to detect (observed) brightness of extraneous light (electron beam diffraction) an output of the detector, a ratio (part of the display fraction in the display monitor) of strip-like non-display areas and strip-like display areas generated (bar-like chrystal) in a display screen (column 16, lines 37, and column 17, lines 4-23).

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki ('4887) in view of Miyazima (US Pub. No: 2002/0171086 A1).

(1) Regarding claim 11:

Note that Yamazaki ('4887) teaches a cathode supply line but Yamazaki does not teach the first wiring has a light shielding function.

However, Miyajima in the same field of endeavor teaches a first wiring (i.e. data line) has a light shielding function [0036], [0127].

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of cathode supply line comprised a light shielding function as taught by Miyajima in to the El display system of Yamazaki so that the cathode signal line could have a shielding function. In this configuration the system would provide a high quality EL display panel with high resolution and improved reliability (Miyajima, [0004]).

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (4887) and Yamazaki ('5549) in view of Miyazima (US Pub. No: 2002/0171086 A1).

Regarding claim 17:

Note that Yamazaki ('5549) does not disclose wherein the anode supply line is arranged to perform a light-shielding function for a circuit forming section of the source driver IC chip.

However, Miyajima in the same field of endeavor teaches a supply line (i.e. supply line corresponding to data line) is arranged to perform a light-shielding function for a circuit forming section of the driver IC chip [0036], [0127].

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of supply line as taught by Miyajima in to the EI display system of Yamazaki ('4887) as modified by Yamazaki ('5549) so that the anode supply line could be arranged to perform a light-shielding function for a circuit forming section of the source driver IC chip. In this configuration the system would provide a high quality EL display panel with high resolution and improved reliability (Miyajima, [0004]).

Response to Arguments

8. Applicant's arguments with respect to claims 1 have been considered but are moot in view of new ground of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

10. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Shaheda Abdin whose telephone number is (571) 270-1673.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard HJerpe could be reached at (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pari-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shaheda Abdin

07/22/2010

/Richard Hjerpe/

Supervisory Patent Examiner, Art Unit 2629